Packaging technology enabling flexible optical interconnections

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ABSTRACT

This paper reports on the latest trends and results on the integration of optical and opto-electronic devices and interconnections inside flexible carrier materials. Electrical circuits on flexible substrates are a very fast growing segment in electronics, but opto-electronics and optics should be able to follow these upcoming trends. This paper presents the back-thinning and packaging of single opto-electronic devices resulting in highly flexible and reliable packages. Optical waveguides and optical out-of-plane coupling structures are integrated inside the same layer stack, resulting in complete VCSEL-to-PD links with low total optical losses and high resistance to heat cycling and moisture exposure.

Keywords: Opto-electronic packaging, flexible, thin chip, VCSEL, optical interconnect, embedding

1. INTRODUCTION

Light as a transmission medium for data communication has proven its success for many years. Over long distances like intercontinental and intercity links, optical interconnects have been the obvious choice due to the low propagation losses and high bandwidth. Over short distances, optical data communication on board has drawn a lot of attention and has proven to bring a solution to the emerging bottle necks of electrical interconnects, but adaption of this technology on a commercial scale has still not been conveyed. As the demonstrated performance of optics on board is higher every year, the adaption in the industry is still predetermined for niche applications.

This paper addresses the introduction of on-board optical communication in one of the fastest growing market segments in electronics today: the flexible substrate electronics. By making the optical interconnects and every accompanying active and passive feature very thin and flexible, we can integrate everything in a thin bendable foil. This opens a world of opportunities in portable and wearable applications were flexible electronics are already dominating today. In automotive, avionics, aero-space and medical applications, optical fiber communication and flexible electronics have made their break-through long time ago, mainly driven by the low weight and compactness of both and the immunity to electromagnetic interference and reliability in harsh environments of optics. The flexible optical interconnections presented in this paper combine the electrical and optical network into one system.

Light is presented here as the carrier of bit data, but in an analog point of view, light can be used for sensing a wide range of chemical, biological and physical parameters. Optical sensor systems have shown some main advantages over their electrical counterparts with a large growth in this research area as a consequence. As sensors often need to be as compact and unobtrusive as possible, the high level of integration reached in this PhD work can significantly reduce the size, measurement point pitch and cost of existing optical sensors.

The integration of opto-electronics, optical waveguides and coupling structures in a 150 μm thin flexible foil presented in this paper can not only find its application in flexible electronics and optical sensors, but brings an additional value to the state-of-the-art of existing on-board rigid interconnects discussed above. Namely, the high level of integration can significantly reduce or even eliminate the footprint of the interconnections, the mechanical flexibility can improve the reliability, the thinness of the foil enables 3D stacking of interconnects and the stand-alone nature of the optical link foil can fasten up the industry acceptance of optics on-board.

2. THINNING OF OPTO-ELECTRONIC DEVICES

Commercially available GaAs opto-electronic components are too thick to be embedded inside a thin foil. We present a backside mechanical thinning process for individual dies for the realization of ultra thin (20 µm) optoelectronic components. The mechanical thinning of single die GaAs opto-electronic components has never been reported before. Therefore the properties of the thinned dies are carefully characterized. The thinning process is described more in detail in [1].

For massive production of ultra thin chips in the IC market, the total thickness variation tolerance is assumed to be 1 µm. Figure 1 (left) shows the backside profile measurement with a non-contact profilometer WYKO of a polished 1 x 4 VCSEL array. A thickness variation of 1.6 µm over the whole chip can be observed after polishing, which is near the mass production tolerances. Figure 1 (right) shows the thickness profile over the length and width axis of the VCSEL array after thinning.

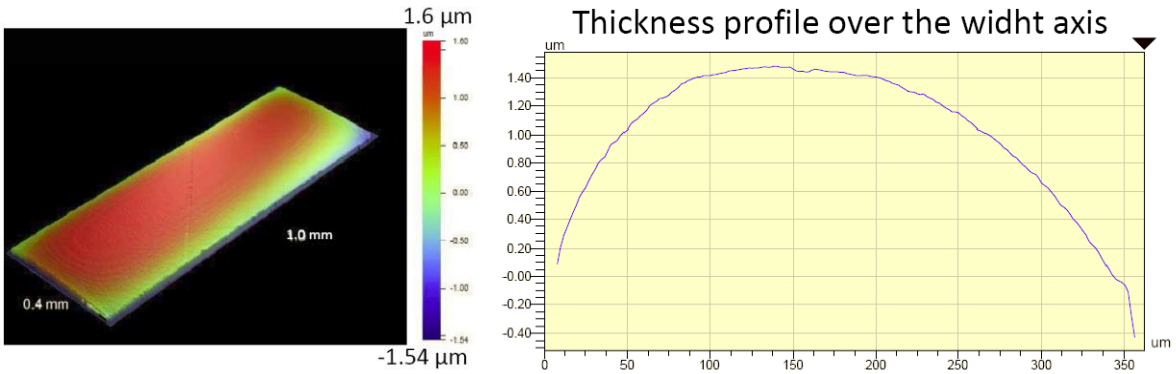


Figure 1: Backside profile measurement with a non-contact profilometer WYKO of a thinned 1 x 4 VCSEL array (left) and the thickness profile over width axis (right).

The chip strength is directly related to the surface roughness of the backside [2]. Backside roughness induces micro-cracks and internal stress which is even more significant when the thin dies will be bended, so minimized roughness is preferred. Figure 2 (left) shows a backside roughness measurement with a non-contact profilometer WYKO of a lapped (left) and a polished (right) 1 x 4 VCSEL array on an area of 200 x 200 µm ^{2}. After polishing, an Rms roughness of 10 nm is measured at the backside, resulting in a very smooth surface with low internal stress. The roundness of the edges of the dies has been minimized (see Figure 2 right) by the right choice of mounting wax during the thinning process.

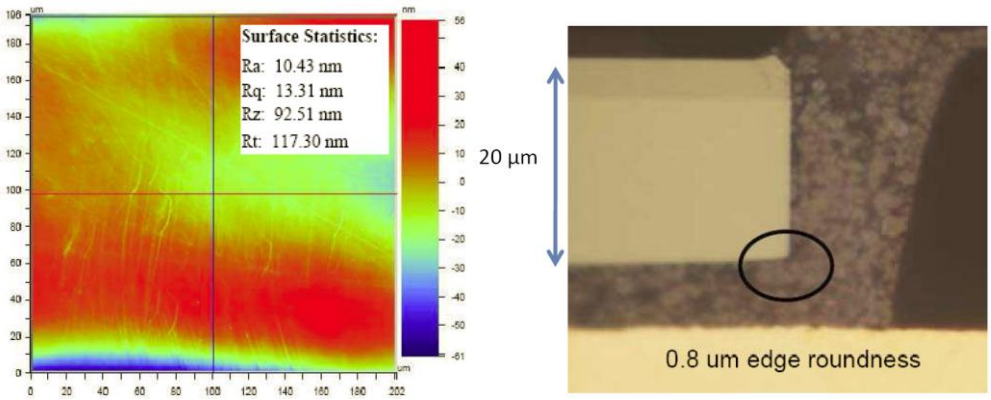


Figure 2: Backside roughness measurement with a non-contact profilometer (WYKO) of a thinned 1 x 4 VCSEL array (left) and the edge roundness (right).

To prove that the characteristics of the VCSEL do not change due to the thinning process, the VI curves of VCSEL's and Photodiode were measured before and after thinning. No differences were measured. To monitor the optical behavior of the VCSEL's, we defined the current threshold of each exited mode. These thresholds were compared for un-thinned and thinned VCSEL's. The results are shown in Figure 3. Again no significant differences were measured. This allows us to state that the presented thinning process for opto-electronic chips does not influence the characteristics of those chips.

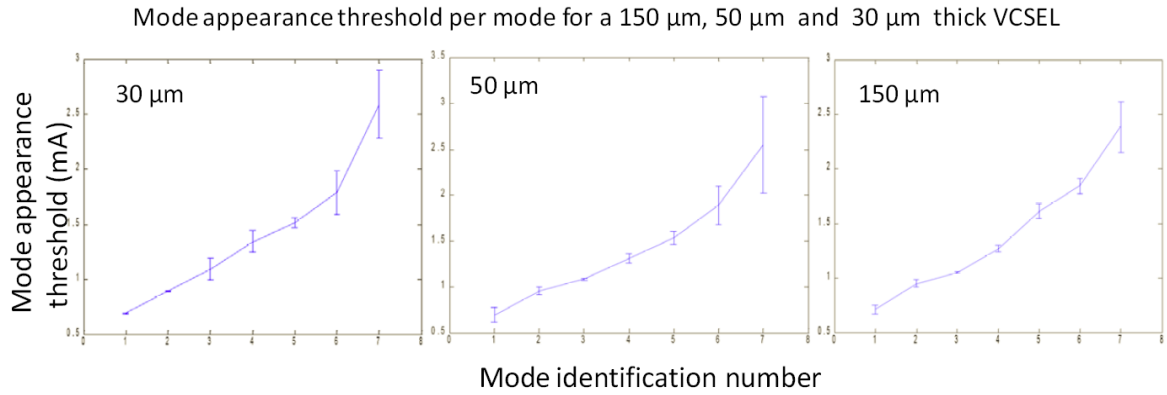


Figure 3: Mode appearance threshold per mode for a 150 µm , 50 µm and 30 µm thick VCSEL

3. FLEXIBLE OPTICAL INTERCONNECTIONS

The embedding of the thinned opto-electronic components in a thin foil foil has been realized with Truemode Backplane Polymer™ [3]. Figure 4 shows the schematic overview of the process flow used to embed thinned VCSEL and PD arrays (20 µm thick) in the cladding layer of the optical waveguides.

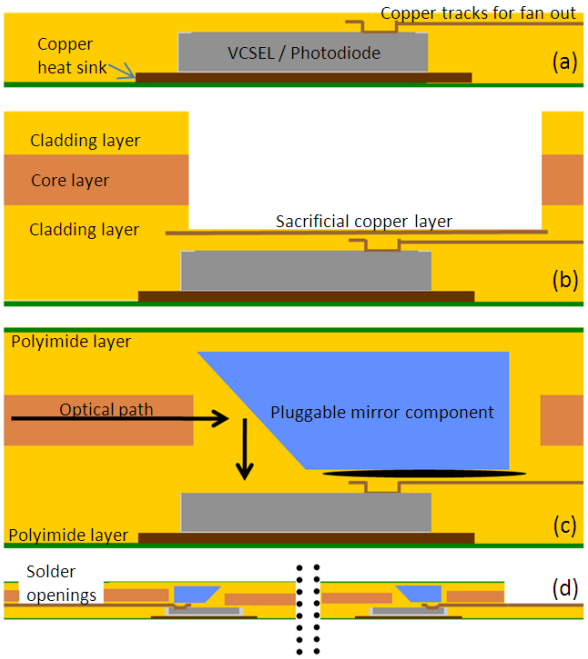
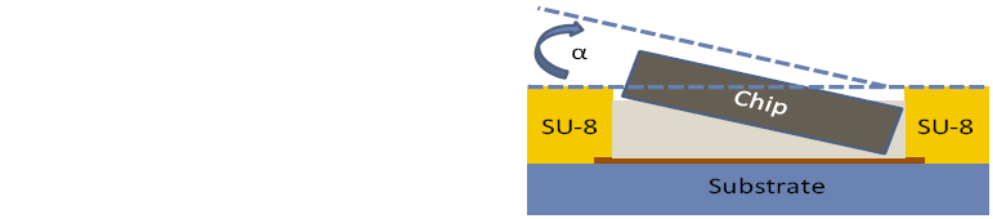
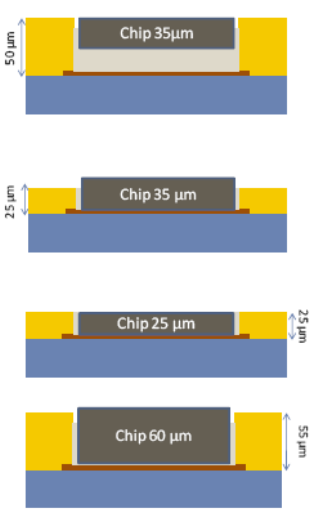


Figure 4: Schematic overview of the process flow for the production of an active flexible opto-electrical link.

For planarization reasons, the VCSEL's and Photodiodes are placed in a cavity inside the under cladding layer. The cavities are laser ablated (KrF Excimer laser; 248 nm wavelength) because of the high-accuracy-needs for the dimensions of the cavity. The cavity must be obviously larger than the die, but cannot be too large because the cavity must perform passive alignment of the die. This way a 10µm positioning accuracy of the die can be obtained. Fine pitch die placers can even lower this accuracy to several microns. In between the under cladding layer and the PI layer, a metal island is deposited. This acts as a heat sink for the active components and also as a laser stop. This way we achieve good depth control of the cavity and fast processing.

The active components are mounted inside the cavity with a low temperature curable adhesive. The adhesive needs to be heat conductive but not electrical conductive and needs to show very low viscosity to fill the whole cavity with a thin adhesive film. To reach the high alignment requirements and coupling efficiencies, it is necessary that the die is perfectly leveled with the substrate surface and not tilted. Figure 5 gives an overview of the chip tilt after mounting in several cases of embedding layer thickness and chip thickness. It is absolutely necessary to keep the embedding layer thinner or equal to chip thickness to achieve acceptable chip tilt.





	VCSEL	Photodiode
Population (pcs)	4	4
Average α (degrees)	1.2	1.1
Standard deviation α (degrees)	0.4	0.6

	VCSEL	Photodiode
Population (pcs)	3	4
Average α (degrees)	0.6	0.5
Standard deviation α (degrees)	0.3	0.2

	VCSEL	Photodiode
Population (pcs)	9	8
Average α (degrees)	0.2	0.1
Standard deviation α (degrees)	0.3	0.3

	VCSEL	Photodiode
Population (pcs)	8	7
Average α (degrees)	0.4	0.3
Standard deviation α (degrees)	0.3	0.3

Figure 5: Tilt angle of a placed and leveled chip inside a laser ablated cavity with respect to the embedding layer surface plane.

In the next step the die is covered with a cladding layer of 10µm to finish the embedding of the die. This layer has proven to be well planarized, meaning that the cavity principle works well. Laser ablated micro-via's are then made to the embedded contact pads and metalized. Metallization is needed to fan out the small pitch contact pads of the embedded VCSEL and Photodiode array's (250 µm pitch) towards larger pitch contact pads (2 mm pitch) on the substrate surface.

The production of waveguides on top of the embedded dies is done with standard lithography and an alignment error in relation to the active area of the opto-electrical components is smaller than 5 µm. A 45 degrees pluggable coupling mirrors are fabricated externally in flexible Polyimide material and embedded in the flexible optical foil on top of the embedded opto-electronics.

The whole structure is then again covered with a cladding layer to cover the embedded component and to obtain final planarization. Figure 6 shows a cross-section of an embedded VCSEL array in Truemode Backplane Polymer™

together with the coupling component and the galvanic interconnection. A more detailed description and evaluation of the fabrication process can be found in [4].

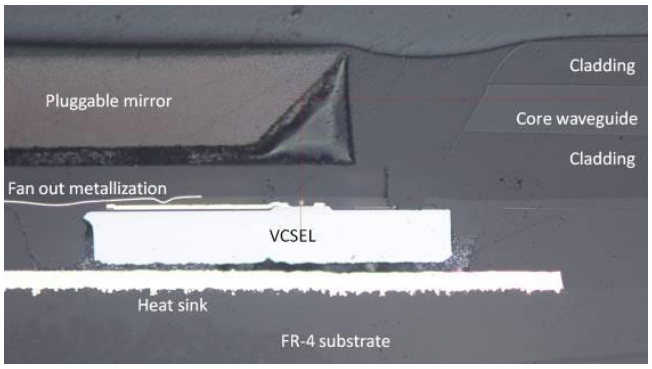


Figure 6: Cross-section of an embedded VCSEL array in the flexible optical link

4. PLUGGABLE MIRROR COMPONENT

This section investigates a new approach of out-of-plane optical coupling by fabricating a discrete component with a 45 degree mirror facet. By creating the mirror component independent from the optical link fabrication, we have full control over the mirror facet roughness and angle. The positioning of the micro-mirror is then purely subject to the accuracy of the mirror component placing. Using a fine pitch pick and place tool, accuracies below 5 µm are achievable. Manual placing of the components results in an accuracy of about 10 µm.

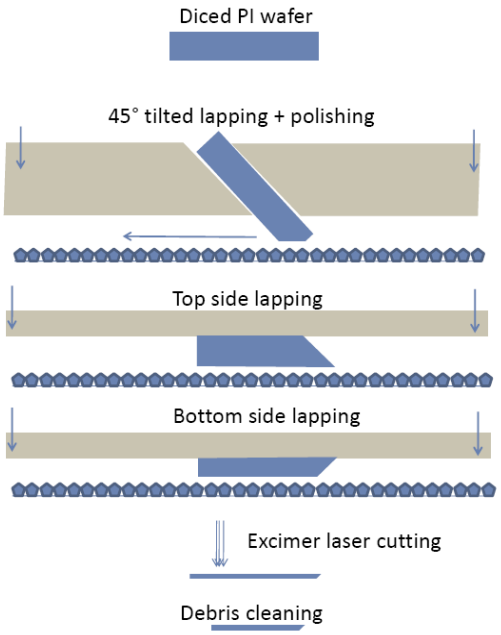


Figure 7: 45 degree mirror plug polishing tool.

A new fabrication technology was developed: 45 degree polishing. The schematic process flow for the 45 degree polishing is shown in Figure 7. The material for the mirror plug is chosen to be Polyimide because of its high thermal stability and flexibility. We start from a mother piece (eg. 1 x 2 cm2) of 500 µm thick PI wafer [5] and clamp it in a special designed polishing tool. It consists of a block of PMMA material which was cut into two pieces at an angle of 45

degrees. These two blocks are then provided with screws to clamp them together and guiding pins to assure that the two blocks can only move horizontally with respect to each other. The PI waferpiece is clamped inside this tool in such a way that it protrudes for a few tens of microns out of the PMMA tool. The whole PMMA polishing tool with the clamped PI waferpiece is then polished on rotation polishing paper and polishing cloths. Large grain polishing paper is used first to make sure the two PMMA blocks of the 45 degree polishing tool are perfectly planar. Lowering the grain size in every next polishing step, reduces the mirror facet roughness to a minimum. The last polishing step is done with a 0.3 µm Al2O3 grain slurry on a soft polishing cloth.

The resulting mirror facet is shown in Figure 8(left), together with a WYKO optical non-contact profilometer plot of the surface (Figure 8(right)). The Ra roughness of the mirror facet, measured on an area of 50 x 50 µm 2 is 13.5 nm, which is well below 1/10 of the used light wavelength (850 nm / 10 = 85 nm). The edges of the 45 degree mirror facet of the motherpiece are a bit rounded due to the polishing and show higher roughness. These side effects are eliminated by lapping the motherpieces at both sides (top and bottom) until it has the aimed thickness of 100 µm (see Figure 7). The lapping process and parameters are the same as for the lapping of the opto-electronics in Section 2. The roughness of the top and bottom side is not important. The wax mounting step however is crucial to assure perfect parallellism of the motherpiece and thus respecting the 45 degree angle of the mirror facet. The last step consists of the laser cutting of the mirror plugs out of the motherpiece. The dimensions of the mirror plug should be 1000 * 2000 µm ^{2}, what means that a motherpiece with a length of 2 cm results in 20 mirror plugs. The proposed fabrication method is thus highly scalable. Figure 9(a) shows the sideview on the mirror plug and 9(b) a close-up on the mirror facet. The softwarebased measurement of the angle shows an angle of 44.46 degrees. Every mirror plug measured this way had a mirror facet angle within a 45 ± 1 degree range.

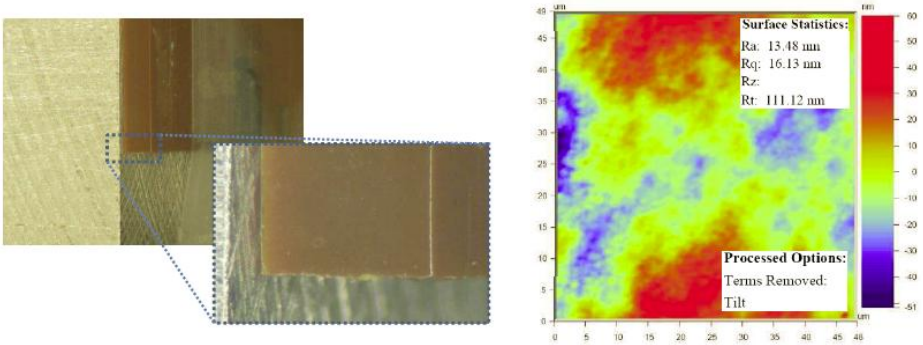


Figure 8: Picture of the mirror facet on the PI motherpiece (left) and a WYKO optical non-contact profilometer plot of the mirror surface (right).

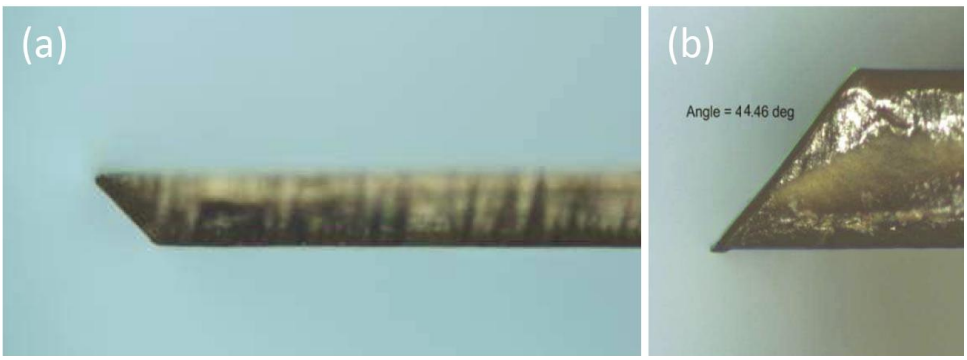


Figure 9: Sideview on a mirror plug (a) and close-up on the mirror facet (b).

For the metallization of the mirror facets, the mirror plugs are mounted on a lowtac tape for handling issues. A vapor deposition process is used to apply a gold layer of 120 nm on top of the mirror facet.

The surface roughness of the mirror facet - though very low - causes optical loss, together with the not perfect reflecting gold layer. To quantify the real coupling losses of the mirror, the following set-up was used: An optical fiber

is positioned horizontal and emits 850 nm wavelength light onto the mirror facet. Another fiber is positioned vertically to collect the mirror reflected light. The ratio between the emitted and the detected light defines the coupling efficiency of the mirror. When using a multimode emitting fiber with core diameter 50 µm (NA = 0.2) and a detecting multimode fiber with core diameter 100 µm (NA = 0.29), we measure a maximum coupling efficiency of 88,5% or a coupling loss of -0.529 dB. When using a singlemode emitting fiber with NA = 0.13 and a detecting multimode fiber with core diameter of 50 µm (NA = 0.13), we measure a maximum coupling efficiency of 89,1% or a coupling loss of -0.502 dB.

5. OPTICAL POWER BUDGET OF THE OPTICAL LINK

The total optical power loss inside the link is subject to many variations in misalignments and layer thicknesses, resulting in a variation of the total optical loss. Therefore it is useful to measure the total optical link loss for as many samples as possible and calculate the average and the standard deviation. Also the best and worst case are interesting to get an idea of the reproducibility of the fabrication process. To measure the total optical loss, we drive a controlled current through the VCSEL and measure the current through the photodiode. We use the information from the measured LI curves of the VCSEL and PD to calculate the conversions from electrical to optical power and vice versa. Figure 10 shows all this information for embedded links. The average total link loss is 6.4 dB.

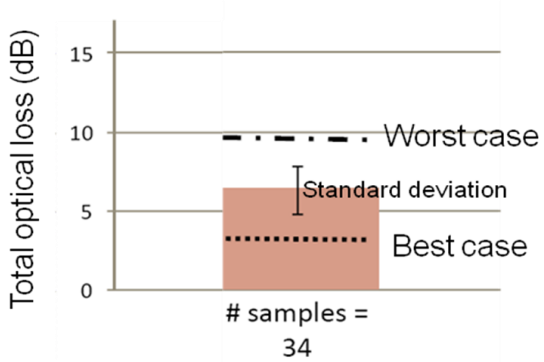


Figure 10: Total optical link loss of the flexible embedded optical links

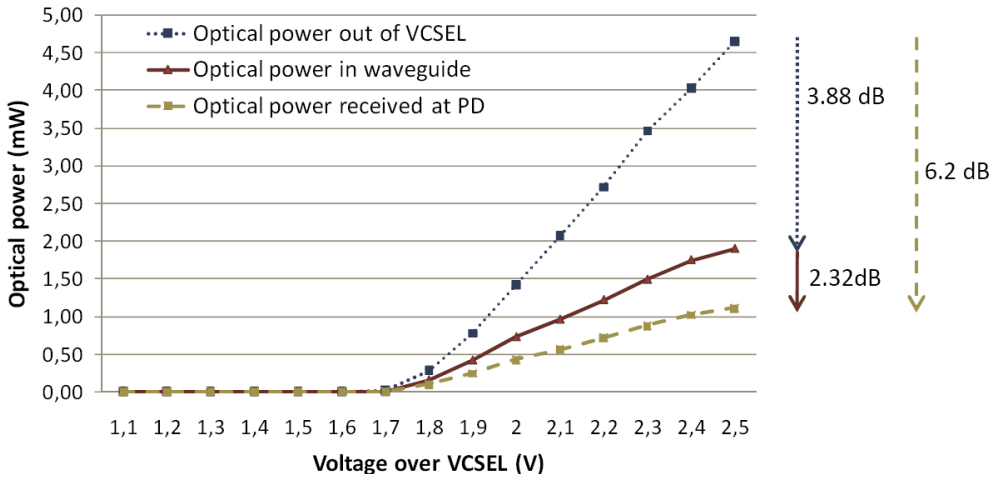


Figure 11: Results from the optical power loss measurement of both halves of the embedded optical link.

The light in the optical embedded link is coupled two times over 90 degrees, once at the VCSEL side and once at the PD side. To define which share each side has in their contribution to the total optical link loss, we sawed the 2 cm long waveguide link into two parts of 1 cm. The end facets of the waveguides were polished to minimize their roughness.

Consecutively we measured the two optical half link losses. For the VCSEL side, a 62.5 µm core size optical fiber (coupled to optical power meter) was aligned with the waveguide facet, while the VCSEL was current driven. For the PD side, a 50 µm core fiber (coupled to a 845 nm laser diode source) was aligned with the waveguide facet, while the PD current was measured. The measurements are shown in Figure 11. The blue curve represents the optical power coming out the VCSEL. The red curve is the power measured at the end of the waveguide from the VCSEL side. The green curve is the power measured at the photodiode, if the power of the red curve is emitted with the laser diode source inside the start facet of the waveguide at the PD side. Halfway the embedded optical link, we see that about 3.9 dB of the optical power is lost and an additional 2.3 dB in the second half. This matches with the simulations results which predicted that most of optical power loss can be found at the VCSEL side.

Figure 12 shows the crosstalk in neighboring plane waveguides (left), and the crosstalk of neighboring complete optical links with embedded mirror plugs (right). The first measurement was performed by coupling light from a 50 µm core optical fiber (coupled to a 845 nm laser diode source) into one waveguide, and measure the power of the light coming out of the neighboring waveguides by aligning a 62.5 µm core optical fiber (coupled to an optical power meter). The waveguides have a pitch of 250 µm meaning that a waveguide at a distance of 250 µm is the first neighbor and the waveguide at a distance of 500 µm the second neighbor and so on. The total optical link crosstalk was measured by driving current through one VCSEL of a 1 x 4 VCSEL array and measuring the current through the other three PD's on the 1 x 4 PD array. The crosstalk to the closest neighboring link is about -17 dB. This is much higher than the crosstalk of -34dB for the planar waveguides. The difference is most probably caused by the distance between the mirror plug mirror facet and the start of the waveguide. The light pad from the VCSEL to the start of the light confining waveguide is quite long. In this pad, the light is subject to divergence, resulting in light being emitted next to the waveguide, into the cladding layer. In literature, a -30 dB crosstalk is required for high performance optical data buses. We do not reach this requirement with the measured -17 dB.

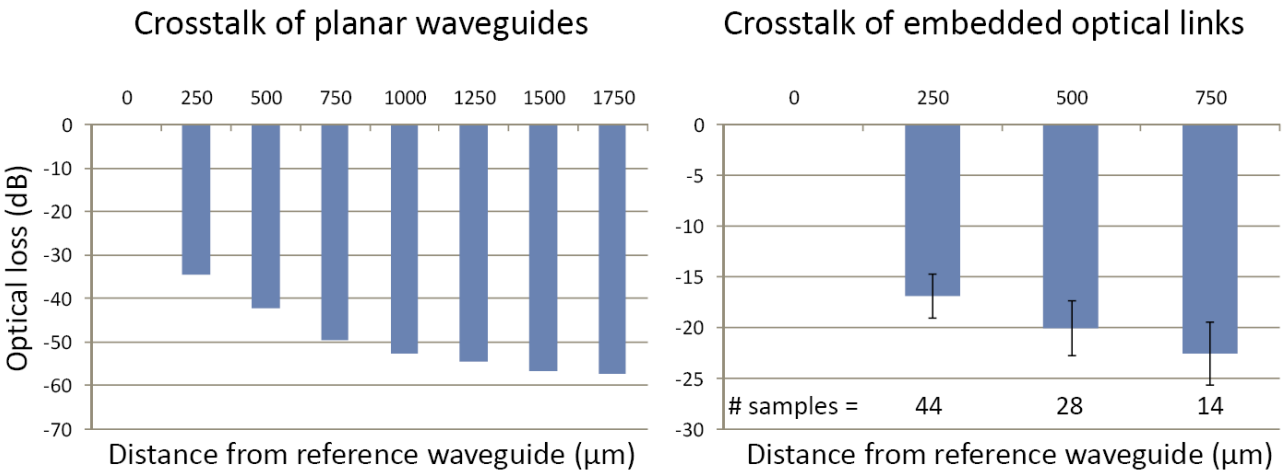


Figure 12: Crosstalk in neighboring plane waveguides (left) and crosstalk in neighboring complete optical links with embedded mirror plugs (right).

6. CHARACTERIZATION OF FLEXIBLE ACTIVE OPTICAL WAVEGUIDE LINKS

Characterization of the embedded optical link foil as a total system was performed by means of the optical power budget, optical crosstalk (see Section 5), high-frequency behavior, mechanical flexibility and reliability. The investigation on the flexible behavior taught us that the flexible optical waveguide foil can be bended over 1000 times over a bending radius of 2.5 mm without damaging and without any chance in functionality or VI curve of the VCSEL or PD.

A special electronic design on an rigid optical embedded link was made to do time and frequency domain characterization using standard 50 Ohm test equipment resulting in a clear open eye diagram at 1.2 Gb/s. The reliability of the flexible optical link was investigated through storage, heat cycling and humidity tests. Temperature cycling and

humidity cycling was performed on both rigid optical links on FR-4 and on flexible optical links. The rigid optical links delaminated from the FR-4 substrate when the temperature reached -30 ^{o}C and their total optical losses increased with the humidity exposure time. The flexible optical links did not degrade at all after 100 temperature cycles between -40^{o}C and + 125^{o}C and after 1000 hours at 85 ^{o}C at a relative humidity of 85 %. More detailed description of these results can be found in [4].

7. CONCLUSIONS

The technology to thin down commercially available opto-electronic components is described in detail in [1] and briefly summarized in this paper. The characterization of this thinning technology was described in detail. The ultra thin (20 µm) opto-electronic components showed the flatness of the chip backside below 2 µm over the complete chip, a very low surface roughness of the chips backside substrate of about 10 nm rma, measured on an area of 200 x 200 µm 2. The edge roundness is limited to 0.8 µm. The optical and electrical characteristics of VCSEL's was compared before and after thinning, showing that the thinning process does not influence the components characteristics.

The fabrication of completely flexible active optical links by embedding of the abovementioned thin dies is briefly summarized in this paper but in detail in [4]. The chip tilt inside the package has been minimized below 1 degree. A highly scalable fabrication process for the realization of pluggable mirrors is presented and characterized, showing a very smooth mirror facet and highly reproducible facet angle.

The embedded optical links have a total optical link loss of 6.5 ± 2 dB and measurements and simulations showed that the coupling at the VCSEL side has the largest contribution to the total loss. The crosstalk between 2 neighboring plain flexible waveguides is -34 dB and the crosstalk between two neighboring VCSEL-to-PD links is -17 dB. A High frequency proof-of-principle measurement showed a clear open eye diagram at 1.2 Gb/s. Finally, humidity cycling for 1000 hours at 85%r.h./85°C and temperature cycling from -40°C to 125°C showed to have no influence on the performance of these flexible optical links.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

1. E. Bosman, G. Van Steenberge, N. Hendrickx, P. Geerinck, J. Vanfleteren and P. Van Daele. Fully embedded optical and electrical communication in flexible foils. Proceedings IMAPS European Microelectronics and Packaging Conference, Rimini, Italy, Jun 2009.
2. Hiep Pham and Chang-Hwang Hua. Strength Improvement for the GaAs Thin Wafer. In International Conference on Compound Semiconductor, 2003.
3. www.exxelis.com Truemode Backplane™ Polymer data sheets
4. E. Bosman, G. Van Steenberge, J. Missine, B. Van Hoe and P. Van Daele. Packaging of opto-electronic devices for flexible applications. Proceedings of SPIE Photonics West Conference, San Francisco, US, Jan 2010.
5. OptiComp Networks Inc. http://www.opticomp.com.
6. IWT project FAOS. http://intecweb.intec.ugent.be/faos/.
7. Photonic Skins For Optical Sensing, "Phosfos". http://www.phosfos.eu/